IN THE DRAWINGS:

Attached Replacement Sheet 1 includes changes to Figure 1. Previously, Figure 1 listed element 140 twice. The Replacement Sheet now is corrected to read element 100 for the general designation.

Attachment: Replacement Sheet

REMARKS/ARGUMENTS

The Applicants originally submitted Claims 1-21 in the application. In a previous response, the Applicants amended Claim 14 to correct an antecedent problem. In the present response, the Applicants have not amended, canceled or added any claims. Accordingly, Claims 1-21 are currently pending in the application.

I. Formal Matters

The Applicants submit a Replacement Sheet including Figure 1. As noted above, the Replacement Sheet corrects an error with the previous submission. The general designation of Figure 1 now reads element 100 rather than element 140.

II. Rejection of Claims 1, 5, 8, & 12 under 35 U.S.C. §102

The Examiner has rejected Claims 1, 5, 8, & 12 under 35 U.S.C. §102(e) as being anticipated by U.S Patent No. 6,737,920 to Jen, *et al.* As the Examiner is no doubt aware, anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference; the disclosed elements must either be disclosed expressly or inherently and must be arranged as in the rejected claims. The Applicants respectfully disagree with the Examiner's rejection since Jen does not teach a phase-error suppressor for use with a plurality of transistors having a common source coupled to a current generator and configured to receive signals at a frequency as recited in independent Claims 1 and 8. More specifically, Jen does not teach an inductor coupled between the common source and the current generator and *causing the inductor to*

resonate proportionally to the frequency of the received signals with a first capacitance associated with the plurality of transistors to suppress a phase-error with the received signals.

Jen provides a matching capacitance circuit to offset a parasitic capacitance, Cgd, found in a gain cell to compensate for the Miller Effect from the parasitic capacitance. Jen discloses a gain cell operable in a variable gain amplifier and including transistors M1 and M2 that have a common-source node. (*See* column 3, lines 49-64 and Figure 5B.) NMOS transistors M3 and M4 are connected as capacitors equal to the parasitic capacitance, Cgd, in the transistors M1 and M2 to cancel the Miller Effect of the parasitic capacitance, Cgd. (*See* column 3, lines 59-63 and Figure 5B.) Additionally, an inductor, Ls, is coupled to the common-source node of the differential pair M1, M2, to resonate out all the associated capacitances and produce a high-impedance node. (*See* column 4, lines 56-59.)

Jen does not teach an inductor coupled in series between a common source and a current generator to resonate proportionally at a frequency of received signals with a first capacitance associated with a plurality of transistors to suppress a phase-error with received signals as recited in independent Claims 1 and 8. On the contrary, the inductor Ls of Jen is configured to resonate out associated capacitance with the differential pair M1 and M2. (*See* column 4, lines 56-59.) Jen does not teach that the inductor Ls is configured to resonate **proportionally with** the associated capacitance of M1 and M2 **at a frequency of received signals**. More specifically, the Applicants do not find where Jen discloses the inductor Ls is configured to resonate proportionally at a frequency of received signals with a capacitance associated with M1 and M2 to suppress a phase-

error with received signals. Thus, Jen does not teach the inductor as presently claimed in independent Claims 1 and 8.

Therefore, Jen does not disclose each and every element of independent Claims 1 and 8. As such, Jen does not anticipate independent Claims 1 and 8. Since Claims 5 and 12 are dependent on Claims 1 and 8, these claims are also not anticipated by Jen. Accordingly, the Applicants respectfully request the Examiner to withdraw the §102(e) rejection with respect to Claims 1, 5, 8 and 12 and allow issuance thereof.

Furthermore, specifically addressing dependent Claims 5 and 12, Jen does not teach a capacitor coupled to the inductor and in parallel to the current generator, wherein the capacitor shunts the inductor to ground at a selected radio frequency (RF). Jen does teach a switched variable capacitor, Cs, in parallel with the combination of the inductor Ls and a current source (IBias). (*See* Figure 5C.) The switched variable capacitor Cs, however, is not used to shunt the inductor to ground. Instead, the switched variable capacitor Cs is used to adjust the tuning frequency at the common-source node for noise rejection at the proper frequency. (*See* column 4, lines 62-65.) As evident from Figure 5C, the switched variable capacitor Cs is not employed to shunt the inductor Ls to ground. Accordingly, Jen also does not teach the subject matter of dependent Claims 5 and 12.

III. Rejection of Claims 2-4, 6, 7, 9-11, and 13-21 under 35 U.S.C. §103

The Examiner has rejected Claims 2-4, 6, 7, 9-11, and 13-21 under 35 U.S.C. §103(a) as being unpatentable over Jen in view of Sano, *et al.* As the Examiner is no doubt aware, determination of obviousness requires consideration of the invention considered as a whole; the

inquiry is not whether each element exists in the prior art, but whether the prior art made obvious the invention as a whole. Furthermore, to establish a *prima facie* case of obviousness, three basic criteria must be met including the cited references must teach or suggest all the claim limitations.

As noted above, Jen does not teach an inductor coupled in series between a common source and a current generator to resonate proportionally at a frequency of received signals with a first capacitance associated with a plurality of transistors to suppress a phase-error with received signals as recited in independent Claims 1 and 8. Additionally, the Applicant does not find where Jen even refers to frequency of received signals and coupling an inductor to resonate with a first capacitance associated with a plurality of transistors to suppress any phase-error of the received signals. Instead, Jen is concerned with cancelling parasitic impedance, Cgd, of a differential pair of transistors, M1 and M2, in an amplifier in a gain cell of a variable gain amplifier. (*See* column 3, lines 53-55 and lines 60-63, and column 4, lines 17-23.) For noise rejection, Jen proposes using a switched variable capacitor, Cs. (*See* column 4, lines 62-64 and Figure 5B.) Thus, Jen does not teach or suggest an inductor coupled in series between a common source and a current generator to resonate proportionally at a frequency of received signals with a first capacitance associated with a plurality of transistors to suppress a phase-error with received signals.

Sano has not been cited to cure the noted deficiency of Jen but to teach the subject matter of the above noted claims. (See Examiner's action, pages 3-5.) Sano teaches inductors connected to input transistors to operate as feedback impedances instead of the resistors that are conventionally used. (*See* column 2, lines 46-49.) There is no teaching in Sano to use these inductors to resonate proportionally at a frequency of received signals with a first capacitance associated with a plurality of

transistors to suppress phase-error. Instead, Sano uses the inductors because there is no dc voltage drop across them and the full supply voltage is applied to the transistors and the load resistors of the mixer. (*See* column 2, lines 51-52.)

Thus, the cited combination of Jen and Sano fails to teach or suggest an inductor coupled in series between a common source and a current generator to resonate proportionally at a frequency of received signals with a first capacitance associated with a plurality of transistors to suppress a phase-error with received signals as recited in independent Claims 1 and 8 and their dependent claims, when considered as a whole. Accordingly, the cited combination also does not teach or suggest an inductor, coupled between a common source and a current generator configured to resonate proportionally to a frequency with a first capacitance associated with a plurality of transistors to suppress a phase-error between in-phase and a quadrature-phase signals as recited in independent Claim 15. As such, the cited combination does not provide a *prima facie* case of obviousness of independent Claims 1, 8 and 15 and Claims 2-4, 6, 7, 9-11, 13-14 and 16-21 which depend thereon, respectively. Claims 2-4, 6, 7, 9-11, and 13-21, therefore, are not unpatentable in view of Jen and Sano and the Applicants respectfully request the Examiner to withdraw the §103(a) rejection of these Claims and allow issuance thereof.

Specifically regarding dependent Claim 19 which includes a capacitor coupled to an inductor and in parallel to a current generator, wherein the capacitor shunts the inductor to ground at a selected radio frequency (RF). As noted above regarding dependent Claims 5 and 12, Jen does not teach this capacitor as claimed but teaches a switched variable capacitor Cs in parallel with an inductor Ls in series with a current source. Jen also does not suggest the claimed capacitor as

evident from Figure 5C, wherein the switched variable capacitor Cs of Jen cannot be used to shunt the inductor Ls to ground. Accordingly, Jen also does not teach or suggest the subject matter of dependent Claim 19.

Sano has not been cited to teach or suggest such a capacitor as claimed and the Applicant does not find where Sano cures this deficiency of Jen. As such, the cited combination of Jen and Sano also does teach or suggest each element of dependent Claim 19.

Furthermore, regarding dependent Claims 7 and 14, the Examiner recognizes that Jen does not teach or suggest wherein the signals are four periodic local oscillator signals having a 90 degree phase difference. To cure this deficiency, the Examiner cites column 2, lines 33-35 of Sano. (*See* Examiner's Action, page 5.) The Applicants do not find a teaching or suggestion in this cite or throughout Sano that cures the noted deficiency of Jen. For example, referring to Figure 1, the inductors 15, 19, of Sano are coupled to the input transistors 7, 9, of a balanced amplifier to provide feedback for the balanced amplifier portion of the circuit. Accordingly, the Applicants respectfully request the Examiner to indicate where Sano discloses the subject matter of dependent Claims 7 and 14.

IV. Conclusion

In view of the foregoing remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-21.

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 08-2395.

Respectfully submitted,

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